REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-2 and 4-17 are pending, with Claim 3 canceled and Claims 1-2 and 4-17 amended by the present amendment.

In the Official Action, Claims 1-17 were rejected under 35 U.S.C. § 102(e) as being anticipated by Solt et al. (U.S. Patent No. 6,988,237, hereinafter "Solt").

The specification is amended to correct a typographical error. Claims 1-2 and 4-17 are amended to more clearly describe and distinctly claim Applicants' invention. Support for this amendment is found in Applicants' originally filed specification.[1] No new matter is added.

Claim 1 is directed to a semiconductor device that includes, *inter alia*, an error checking and correcting unit (ECC unit) configured to output a test pattern to the data memory, and to generate, from a Hamming matrix which meets a given condition and a transposed matrix of the test pattern, an error checking and correcting code (ECC code) as generated code data corresponding to the stored data and configured for use in checking bit errors of all cells in the data memory. Independent Claim 14 is directed to a method that includes generating an ECC code from a Hamming matrix and a transposed matrix of a test pattern.

Solt describes an integrated circuit (IC) having a memory with plural memory lines, each memory line including plural data cells and plural error-correction (EC) cells to store an EC bit corresponding to the data bit stored in the data cells. The IC also includes an EC input circuit to generate the EC bits based on the corresponding data bits. The IC also includes an EC output circuit having an EC correction circuit to correct errors in the bits in the data cells

[1] Specification page 11, lines 17-24 and page 15, line 25.

of each of the memory lines in accordance with the bits read from the EC cells of the memory line.[2]

Applicants submit that the ECC code generation of Solt is an example of conventional ECC code generation, as expressed by equation (1) of Applicants' originally filed specification. That is, in Solt, when data is written to memory 106, EC input circuit 108 generates EC bits based on the data bits using an algorithm such as a Hamming code. The EC input circuit 108 writes the data bits to the data cells 122 of a memory line 120 in memory 106 and writes the EC bits to the EC cells 124 of that memory line 120.[3] However, Solt does not disclose or suggest an ECC code generator configured to generate code data required for checking bit errors of all cells in a code memory ***using a Hamming matrix and a transposed matrix of a test pattern***.

MPEP § 2131 notes that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also MPEP § 2131.02. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Because Solt does not disclose or suggest the device of Claim 1 or the method of Claim 14, Solt does not anticipate the invention recited in Claims 1 and 14, and all claims depending therefrom.

[2] Solt paragraph 2, lines 8-23.
[3] Solt column 4, lines 8-14.

Accordingly, in view of the present amendment and in light of the previous discussion, Applicants respectfully submit that the present application is in condition for allowance and respectfully request an early and favorable action to that effect.

Respectfully submitted,

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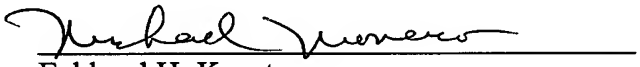

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